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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,127	02/27/2004	Wataru Kikuchi	Q80142	4673

23373 7590 03/13/2006

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/787,127	Applicant(s) KIKUCHI ET AL.	
	Examiner Monica Lewis	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *4-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 12-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/05;10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed December 16, 2005.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no disclosure of the package pins comprising additional pins.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba (U.S. Publication No. 2001/0040793) in view of Forthun (U.S. Patent No. 6,473,308).

In regards to claim 1, Inaba discloses the following:

a) a substrate (2) having first and second surfaces opposite to each other, and first and second semiconductor chips (3) each of which has a mounting surface provided with a plurality of chip pins (8), the first and second semiconductor chips being mounted on the first and the second surfaces of the substrate, respectively, so that the mounting surfaces are faced to each other with the substrate interposed therebetween (For Example: See Figure 2).

In regards to claim 1, Inaba fails to disclose the following:

a) a plurality of chip pins arranged in a predetermined pattern.

However, Forthum discloses a plurality of chip pins arranged in a predetermined pattern (For Example: See Column 2 Lines 32-46). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include a plurality of chip pins arranged in a predetermined pattern as disclosed in Forthum because it aids in providing an electrical connection among the components (For Example: See Column 5 Lines 9-57 and Column 6 Lines 1-15).

Additionally, since Inaba and Forthum are both from the same field of endeavor, the purpose disclosed by Forthum would have been recognized in the pertinent art of Inaba.

In regards to claim 2, Inaba discloses the following:

a) the substrate has a plurality of package pins (7) corresponding to the chip pins, respectively, and formed on the first or the second surface in an area different from a chip mounting area where the first or second chip is mounted (For Example: See Figure 3 and Paragraphs 56-62).

In regards to claim 3, Inaba fails to disclose the following:

a) the package pins are arranged in a pattern identical to the predetermined pattern.

However, Forthum discloses package pins that are arranged in a pattern identical to the predetermined pattern. (For Example: See Column 2 Lines 32-46). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include package pins that are arranged in a pattern identical to the predetermined pattern as disclosed in Forthum because it aids in providing an electrical

connection among the components (For Example: See Column 5 Lines 9-57 and Column 6 Lines 1-15).

Additionally, since Inaba and Forthum are both from the same field of endeavor, the purpose disclosed by Forthum would have been recognized in the pertinent art of Inaba.

In regards to claim 12, Inaba fails to disclose the following:

a) the arrangement of package pins is based on the predetermined pattern.

However, Forthum discloses package pins that are arranged based on a predetermined pattern. (For Example: See Column 2 Lines 32-46). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include package pins that are arranged based on a predetermined pattern as disclosed in Forthum because it aids in providing an electrical connection among the components (For Example: See Column 5 Lines 9-57 and Column 6 Lines 1-15).

Additionally, since Inaba and Forthum are both from the same field of endeavor, the purpose disclosed by Forthum would have been recognized in the pertinent art of Inaba.

In regards to claim 13, Inaba fails to disclose the following:

a) the package pins comprise pins arranged according to the predetermined pattern and additional pins.

However, Forthum discloses package pins that comprise pins that are arranged based on a predetermined pattern and additional pins (For Example: See Column 2 Lines 32-46 and Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include package pins that comprise pins that are arranged based on a predetermined pattern and additional pins as disclosed in

Forthum because it aids in providing an electrical connection among the components (For Example: See Column 5 Lines 9-57 and Column 6 Lines 1-15).

Additionally, since Inaba and Forthum are both from the same field of endeavor, the purpose disclosed by Forthum would have been recognized in the pertinent art of Inaba.

In regards to claim 14, Inaba discloses the following:

a) the chip pins of the first semiconductor chip arranged on the substrate so as to be a mirror-image of the chip-pins of the second semiconductor package (For Example: See Figure 2).

6. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba (U.S. Publication No. 2001/0040793) in view of Forthun (U.S. Patent No. 6,473,308) and Matsuura et al. (U.S. Publication No. 2003/0080438).

In regards to claim 15, Inaba fails to disclose the following:

a) the first semiconductor chip and the second semiconductor chip are aligned with one another.

However, Matsuura et al. ("Matsuura") discloses that the first semiconductor chip (10') and the second semiconductor chip (10') are aligned with one another (For Example: See Figure 8). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include the first semiconductor chip and the second semiconductor chip are aligned with one another as disclosed in Matsuura because it aids in providing a module where chips are mounted compactly and reliably (For Example: See Paragraph 10).

Additionally, since Inaba and Matsuura are both from the same field of endeavor, the purpose disclosed by Matsuura would have been recognized in the pertinent art of Inaba.

In regards to claim 16, Inaba fails to disclose the following:

a) the chip pins of the first semiconductor chip and the chip pins of the second semiconductor chip are aligned with one another.

However, Matsuura discloses that the chip pins (71) of the first semiconductor chip and the chip pins of the second semiconductor chip are aligned with one another (For Example: See Figure 8). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include the chip pins of the first semiconductor chip and the chip pins of the second semiconductor chip are aligned with one another as disclosed in Matsuura because it aids in providing a module where chips are mounted compactly and reliably (For Example: See Paragraph 10).

Additionally, since Inaba and Matsuura are both from the same field of endeavor, the purpose disclosed by Matsuura would have been recognized in the pertinent art of Inaba.

Response to Arguments

7. Applicant's arguments filed 12/16/05 have been fully considered but they are not persuasive. Applicant argued that "the Examiner's alleged motivation for modifying Inaba with Forthun is improper and claim 1 is allowable over the Examiner's combination." However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inaba to include a plurality of chip pins arranged in a predetermined pattern as disclosed in Forthum because it aids in providing an electrical connection among the components (For Example: See Column 5 Lines 9-57 and Column 6 Lines 1-15).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

February 27, 2006

Mary Wilczewski
Primary Examiner